In-class questions for Presentation:

*CPU Cache Prefetching: Timing Evaluation of Hardware Implementations*
• Prefetching algorithms have been concerned with three issues: which blocks to prefetch, how many blocks to prefetch, and when to prefetch. The choices made on these issues in its design determine the effectiveness of the cache prefetching, or how well its advantages are maximized and its disadvantages are minimized.

What are possible advantages and disadvantages of a cache prefetching strategy?

• If the following statement is correct, why?

“A cache prefetching strategy that can decrease miss ratio will improve CPU performance (by reducing memory stall time).”

• What is the difference between normal cache miss and partial cache miss (or accordingly true miss ratio and partial miss ratio)?

• What is double ported cache (tag arrays and data arrays)?
• What is write buffer? What is it used for? Can the write buffer be helpful in reducing miss ratio? Why?

• How would the increase of cache size affect the effectiveness of prefetching? Why?

• How would the increase of cache block size affect the effectiveness of prefetching? Why?