

Cadence Verilog Simulation Guide and Tutorial

ECE 4680: Computer Organization

Outline

- Introduction
- Setting up your Working Environment
- Compilation
- Elaboration
- Simulation
- Examples
- LAB Exercises

Introduction

- This guide describes, via a tutorial, how use Cadence Tools to work with Verilog.
- Cadence tools can be accessed from Eng 2360 LAB.
- This guide is presented in three sections:
 1. [How to set up your environment to view the documents and run the simulator tools.](#)
 2. [Executing the Verilog simulator.](#)
 3. [How to visualize the simulation results.](#)

Setting up your Working Environment

- Login to your Linux machine.
 - Use your WSU access ID and password.
- Double click on the “ab1234’s Home” folder on your desktop.
 - (“ab1234” should be your AccessID).
- Click “View” and check “Show Hidden Files”.
- Scroll down to find the .cshrc file.
 - The file is currently Read Only.
 - Right click on the file and choose “Properties”.
 - Go to the “Permissions” tag and check “Owner >Write”.
 - Click “Close”.
 - Now the file can be edited.
- Right click on the file and choose “Open with Text Editor”.
 - This will open the .cshrc file in the text editor.

Setting up your Working Environment (cont...)

- If you can find the following line
`"source /usr/local/etc/ALLSET"`
 comment out it by putting # sign in front of it.
 - like this: `# source /usr/local/etc/ALLSET`
- Add these two lines to the file:
 - `source /opt/cds/class/cds_setup`
 - `source /opt/cds/class/setup_files/vhdl/vhdl_setup`
- Save and close the editor.
- Open a new terminal (by right click on the desktop and choose "Open Terminal") and type the commands:
 - `cd $HOME`
 - `source .cshrc`

Setting up your Working Environment (cont...)

- Create new *directory*, name it *cadence*, under you home directory.
 - `mkdir cadence`
- Create *vhdl* directory under *cadence* directory.
 - `mkdir vhdl`
- Execute the following commands:
 - `cd vhdl`
 - `cp $NCVHDL/cds.lib $CDSVHDL`
 - `cp $NCVHDL/hdl.var $CDSVHDL`
- *Now your environment is ready.*

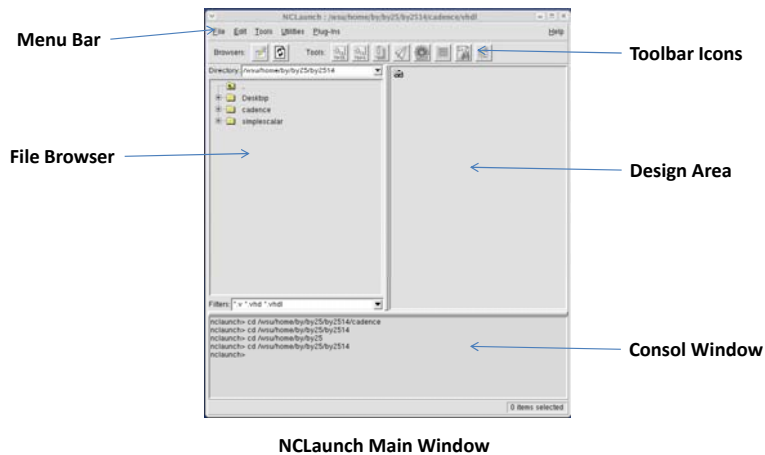
Writing Verilog Code

- You should start by setting up directories for your new code.
 - `cd $CDSVHDL`
 - `mkdir alu`
 - `cd alu`
 - `mkdir src`
- Open a text editor.
 - (Applications → accessories → text editor)
- Go to (http://www.ece.eng.wayne.edu/~nabil/ece4680/labs/lab2_alu.v)
- Copy the code from the page and paste it in the text editor window.
- Change the module name in the code as required.
- Save the file in the `src` directory with the name
 - `<your last name>_alu.v`

Compiling Verilog Code

- On a *terminal*, type the following commands
 - `cd $HOME/cadence/vhdl`
 - `nclaunch &`
- The *nclaunch* command opens the NCLaunch main window.

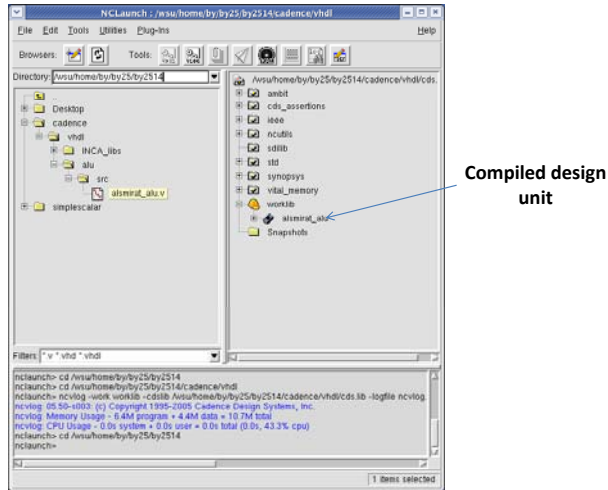
Compiling Verilog Code (cont ...)



Compiling Verilog Code (cont ...)

- Select your Verilog source file from *File Browser area*.
 - *If you can not see it, brows for it.*
- Choose *Verilog compiler* from Tools main menu.
 - The Compile form appears.
 - Press OK. (without changing any thing).
- The results of the compilation appear in the Console Window.
 - If you have errors, read them from the consol window and fix them in the source file using a text editor.

Compiling Verilog Code (cont ...)



Elaborating the Design

- The elaboration process constructs a design hierarchy based on the instantiation and configuration information in the design, establishes signal connectivity, and computes initial values for all objects in the design.
 - *Make the compiled unit ready to use in the simulation*
- Click the plus sign to the left of the *worklib library (vhdl)* in the *Library Browser* to expand it.
- Select the top-level design unit.
- Choose *Elaborator* from the *Tools menu*.
- Press OK. (without changing anything).
- This design hierarchy is stored in a simulation snapshot.
- The snapshot is the representation of your design that the simulator uses to run the simulation.

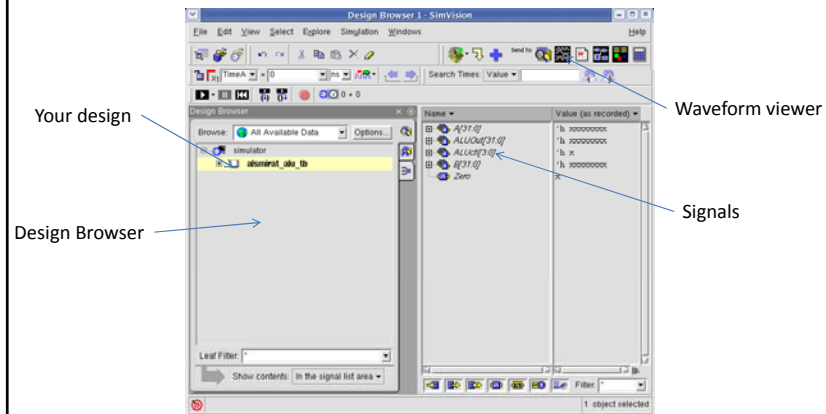
Creating the test bench design

- Open a text editor.
- Go to http://www.ece.eng.wayne.edu/~nabil/ece4680/labs/lab2_alu_tb.v
- Copy the code from the page and paste it in the text editor window.
- Change the module name in the code as required.
- Save the file in the *src* directory with the name
– *<your last name>_alu_tb.v*
- Compile and elaborate the new code.


Simulation with NcSim

- Load the Snapshot into the Simulator.
 - In the *Design Area*, in the *snapshot folder*, select the test bench component.
 - Choose *Simulator* from *Tools Menu*.
 - Press OK

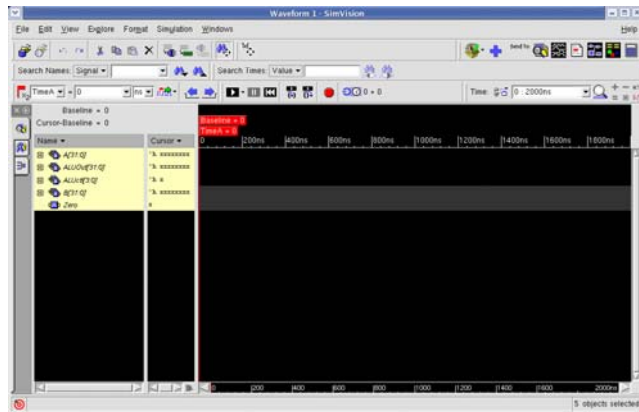
Simulation with NcSim (cont ...)




Simulation with NcSim (cont ...)

- To view signals in SignalScan Waveform Viewer:
 - Select your design from the *Design Browser*.
 - Choose *Signals* from the *Select* menu.
 - Click on the button  in the upper right corner.

Simulation with NcSim (cont ...)



Simulation with NcSim (cont ...)

- Click on the button  on the new window to start simulation.

